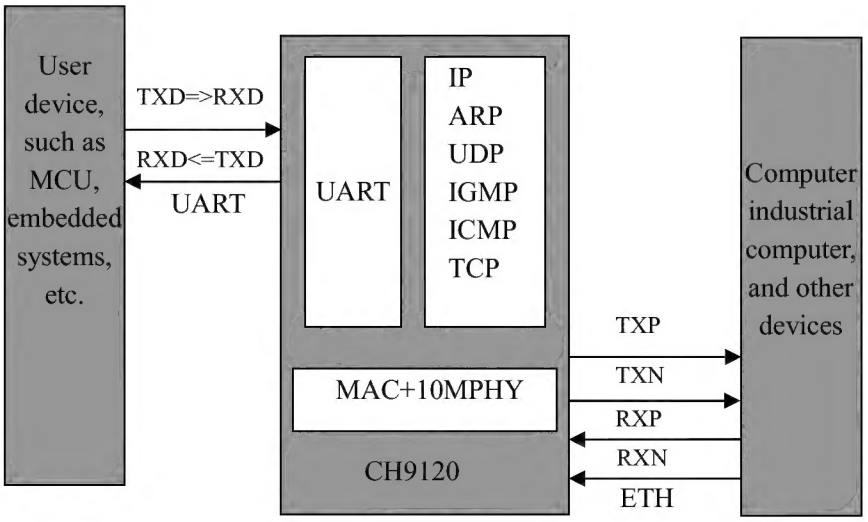
Network and UART Transparent Transmission Chip CH9120

Datasheet
Version: 1B
http://wch.cn

1. Overview

CH9120 is a chip that realizes transparent transmission between network and UART. It integrates TCP/IP protocol stack, which can realize bidirectional transparent transmission between network data packets and serial data. It has 4 working modes: TCP CLIENT, TCP SERVER, UDP CLIENT and UDP SERVER. The baud rate can be up to 921600bps. It can be easily configured by upper computer software or serial commands, which is convenient and quick.

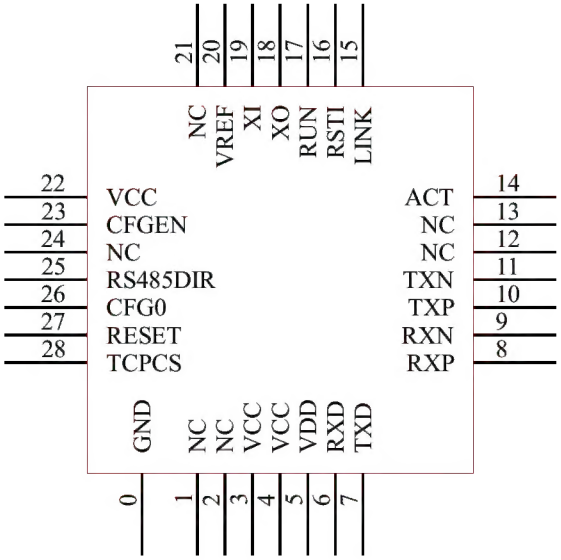
The figure below is a general application block diagram of CH9120.



2. Features

- Internal Ethernet MAC layer and PHY layer
- Realize bidirectional transparent transmission of serial data and network data
- Support 10M, full/half duplex self-adaption Ethernet interface, and compatible with 802.3 protocol
- Support automatic MDI/MDIX line conversion
- Support DHCP automatic access to IP address, and DNS domain name access
- Set the chip working mode, port, IP and other network parameters through upper computer software and serial commands
- Support four working modes: TCP CLIENT, TCP SERVER, UDP CLIENT and UDP SERVER
- Support KEEPALIVE mechanism
- Baud rate range: 300bps ~ 921600bps
- Serial port 3.3V TTL level.

3. Package



Chip	Package	
	Name	Description
CH9120	QFN28	QFN package; 28pins; package body 4x4mm

4. Pins

CH9120 Pin No.	Pin Name	Pin Type	Pin description
0	GND	Power	Ground
3,4,22	VCC	Power	Internal power supply, required to be externally connected with a 0.1uF decoupling capacitor
5	VDD	Power	3.3V working voltage input, externally connected with a 2.2UF decoupling capacitor
6	RXD	Input	UART data input, with built-in pull-up resistor
7	TXD	Output	UART data output, with built-in pull-up resistor
8	RXP	Ethernet signal	Ethernet RXP signal
9	RXN	Ethernet signal	Ethernet RXN signal
10	TXP	Ethernet signal	Ethernet TXP signal
11	TXN	Ethernet signal	Ethernet TXN signal
14	ACT	Output	Ethernet connection communication indicator LED drive pin
15	LINK	Output	PHY connection indication pin, active low
16	RSTI	Input	External reset input, active low
17	RUN	Output	CH9120 running status indication pin, multiplexed as ISP upgrade pin

18	XO	Output	Output of crystal oscillator, required to be connected with an external 32MHz crystal oscillator
19	XI	Input	Input of crystal oscillator, required to be connected with an external 32MHz crystal oscillator
20	VREF	Power	Internal analog circuit power node, required to be connected with an external 1uF decoupling capacitor
23	CFGEN	Input	Network configuration enable pin, detects when power-up, network configuration disabled when at low level. It is suspended by default.
25	RS485DIR	Output	UART RS485 receive/transmit direction control pin
26	CFG0	Input	UART configuration mode set pin, with built in pull-up. If low level is detected, enter UARTconfiguration mode, and exit the mode if high level is detected
27	RESET	Input	Restore factory settings, chip power-on detection, active low
28	TCPCS	Output	Connection status indicator in TCP client mode, low level represents successful connection.
1,2,12,13,21 ,24,	NC	NC	Reserved pins, suspended.

5. Functional Specification

5.1. Functional Description

CH9120 is a chip for transparent transmission between network and UART, which can realize the bidirectional transparent transmission of serial data and network data. It supports 4 working modes (TCP CLEINT/SERVER, UDP CLIENT/SERVER), and the baud rate supported ranges from 300bps to 921600bps. Before use, the network and UART parameters of the chip shall be configured by the upper computer software NetModuleConfig. Exe or the serial command. After the configuration is completed, CH9120 will save the configuration parameters to the internal storage space. And after the chip is reset, CH9120 will work according to the saved configuration value.

The basic parameters of CH9120 include: name, MAC address display, automatic access IP address setting, manual IP address setting (including CH9120 IP address, subnet mask, default gateway), and UART negotiation configuration.

The name is mainly for the convenience of CH9120 module management within the LAN, with the length of not more than 20 bytes. The MAC address field shows the MAC address of the currently selected module. There are two ways for CH9120 to set network parameters. 1) DHCP, that is, it automatically obtains network parameters from the gateway device with DHCP SERVER function; 2) manual setting. UART negotiation configuration function is to enter the serial configuration mode by handshaking through UART, which is disabled by default.

CH9120 port parameters include: network mode, local port, target IP/domain name, destination port, serial port baud rate/data bit/stop bit/parity check bit, network cable disconnection processing, RX packet length, RX packet timeout interval, network connection operation.

The network mode (TCP SERVER/CLIENT, UDP SERVER/CLIENT), destination IP address, and local/destination port are the basic parameters of network communication. And the destination IP address can also be accessed by domain name.

The baud rate ranges from 300bps to 921600bps (the baud rate error of the serial port transmitting signal is

less than 0.5%, and the allowable baud rate error of the serial port receiving signal is not less than 2%). It supports 5/6/7/8 data bits, 1/2 stop bits, odd/even/no parity check, blank 0, and mark 1 check mode.

The network cable disconnection processing means that when the network cable is disconnected, CH9120 actively closes the connection or does not take any action.

The length range of RX packet is 1-512, which means that when the length of CH9120 UART receiving data reaches the set length, CH9120 will immediately package the serial data and send it out via network. The timeout time setting range is 0-200, and the timeout unit is about 5ms. For example, when the timeout is 1, the data length of the serial port receiving buffer does not reach the length of the RX packet, and the serial port does not receive a new one in more than 5ms, the serial port timeout will occur. After the serial port timeout occurs, CH9120 will send the data received by the serial port over the network. When the timeout time is set to 0, the internal hardware timeout mechanism (no new data is received after 4 data times) will be enabled, which is suitable for occasions where real-time requirements are high and large quantities of data are sent and received.

Clear serial port buffer setting refers to how the data received by the serial port is processed before the network connection is established, the data is cleared (discarded) after TCP connection or retained.

5.2. Default Configuration

When CH9120 leaves factory, the network works in TCP CLIENT mode by default. The default parameters related to the network are as follows:

（1） Device IP: 192.168.1.200
（2） Subnet mask: 255.255.255.0
（3） Default gateway: 192.168.1.1
（4） Module port: 2000
（5） Destination IP: 192.168.1.100
（6） Destination port: 1000

UART related default parameters are:

（1） Baud rate: 9600
（2） Timeout: 0
（3） Data bit: 8. Stop bit: 1. Parity check bit: No
（4） Clear serial port buffer: Never

6. Parameters

6.1. Absolute Maximum Value

Critical value or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged.

Name	Parameter description		Min.	Max.	Unit
TA	Ambient temperature during operation	VDD=3.3V	-40	85	℃
TS	Ambient temperature during storage		-55	125	℃
VDD	Supply voltage (VDD connects to the positive power, GND to ground)		-0.4	4.0	V
VIO	Voltage on the input or output pins		-0.4	VDD+0.4	V

6.2. Electrical Parameters

Test conditions: TA=25°C, VDD=3.3V, baud rate: 115200bps)

Name	Parameter description	Min.	Typ.	Max.	Unit
VDD	Supply voltage	2.1	3.3	3.6	V
IPK	Peak current		100		mA
IDD	Current when network receives		25		mA
	Current when network transmits		15		mA
	Current when network is idle		10		mA
VIL	GPIO low level input voltage	0		0.9	V
VIH	GPIO high level input voltage	2.0		VDD	V
VOL	Low level output voltage (5mA/20mA draw current)	0	0.3	0.4	V
VOH	High level output voltage (5mA/20mA output current)	VDD-0.4	VDD-0.3	VDD	V
IUP	Input current at the input terminal of GPIO built-in pull-up resistor	25	60	90	uA
IDN	Input current at the input terminal of GPIO built-in pull-down resistor	-90	-60	25	uA